

## REMARKS

Claims 1, 3, and 5-18 remain in the application with claims 1, 3, 5, 8, 11, 17, and 18 having been amended hereby.

Reconsideration is respectfully requested of the rejection of claims 1, 3, 14, 17, and 18 under 35 U.S.C. 102(e), as being anticipated by *Porter, et al.*

As previously explained, an exemplary embodiment of the present invention is intended to provide a memory device that can be operable in a test mode with a merged data input/output pin in either a first or second data rate. As seen in FIG. 3, the first path circuit includes a transistor 318 that receives a so-called second single data rate signal. Similarly, the second path circuit includes a transistor 338 that is controlled by a so-called first single data rate signal. The first and second single data rate signals are generated by a control signal generator shown in FIG. 4, and the first and second single data rate signals are based upon output clock signals fed to the control signal generator. By controlling these transistors, it is determined whether the first and second data path circuits operate under the single data rate pattern or dual data rate pattern.

*Porter, et al.* relates to a system in which data output paths can have selectable data rates. As shown in FIG. 2, an odd path and an even path are provided to supply data to the output register 102. In other words, two different kinds of data are typically fed to the output register, although they can be the first part of a data word and the second part of the data word. As noted in the double rate operation, the second piece of data is a different piece than the first piece of data. A selection mechanism is connected to the data paths and allows selection of the single or double rate operation. The operation of

this selection mechanism is not discussed in detail. Moreover, contrary to the Examiner's assertion in page 4 of the office action, there is nothing shown in FIG. 2 or at column 2, lines 10-16 of *Porter, et al.* that discloses whether the output is a single data rate pattern or a dual data rate pattern, as determined by the first and second single data rate signals and first and second transmission signal pairs, as in the presently claimed invention. FIG. 2 and the specification at column 2, lines 10-16 of *Porter, et al.* do not disclose this feature of the present invention .

Moreover, this feature of the present invention has now been emphasized in claims 1 and 17 to make it more clear how the first and second single data rate signals are applied with a switching element in the second and first path circuits, respectively, to control the data rates.

In regard to claim 3, it will be noted that element 101 of *Porter, et al.* is disclosed as being a memory and not a control signal generator.

In regard to claims 17 and 18, claim 17 has been amended hereby to specifically recite the structure of the first and second path circuits that are controlled by the second and first single data rate signals.

Accordingly, it is respectfully submitted that the claims are not anticipated by *Porter, et al.*

Reconsideration is respectfully requested of the rejection of claims 5-13, 15, and 16, under 35 U.S.C. 103(a), as being unpatentable in view of *Porter, et al.*

Claims 5-13, 15 and 16 depend from claim 1 which, for the reasons set forth hereinabove, is thought to be patentably distinct over the cited reference and, for at least

those very same reasons, claims 5-13, 15 and 16 are also submitted to be patentably distinct thereover.

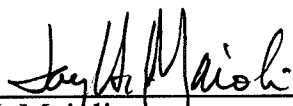
Accordingly, in view of the amendments made to the claims hereby, as well as the above remarks, it is respectfully submitted that a semiconductor memory device operable in a merged data test mode under either a single data rate pattern or dual data rate pattern, as taught by the present invention and as recited in the amended claims, is neither shown nor suggested in the cited reference.

The references cited as of interest have been reviewed and are not seen to show or suggest the present invention, as recited in the amended claims.

Entry of this Amendment is earnestly solicited and it is respectfully submitted that this Amendment raises no new issues requiring further consideration and/or search, because the originally recited structure has simply been set forth in more detail.

Favorable reconsideration is earnestly solicited.

Respectfully submitted,

  
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